Memo

TO: Micah Taylor, Project Lead

FROM: Jeffery Humphrey, Benjamin Efron, Josh Gayso, Thomas Bonatti, Designers

DATE: February 5, 2015

SUBJECT: Milestone V – Datapath Implementation

Any broken components have been fixed and clocked, and the test benches for those components rewritten to adequately test them. We performed integration testing on different sets of components, such as the PC and adder, the Register file and ALU, and the PC adder component with the register file. All known issues with the RTL have been fixed, and the design document has been updated accordingly. Shift right arithmetic (sra) has been removed from our instruction list to be re-implemented as a pseudo-instruction, and the bits that were used for sra and for set less than immediate (slti) are currently being used for branch equal to zero (beqz) and branch not equal to zero (bnez). The RTL testing simulation and the assembler have been completed, and the compiler is nearing completion. All components will be combined into a single testing environment where both assembly and scheme code can be tested for the processor. Once the datapath integration is completed we will have ample time to finish all of our extra features and thoroughly test our processor and make any adjustments we feel would improve it.